

We Claim:

- 1 1. A method, comprising:
2 obtaining, from within a memory system, information to indicate a data mask
3 mapping scheme to be used in a memory module in the memory system; and
4 determining the data mask mapping scheme based on the information.
- 1 2. The method of claim 1, wherein said obtaining includes:
2 sending at least one instruction to the memory module directing the memory
3 module to send the information; and
4 receiving the information from the memory module.
- 1 3. The method of claim 2, wherein said receiving the information from the memory
2 module includes receiving the information from a serial presence detect within the
3 memory module.
- 1 4. The method of claim 3, wherein said receiving the information from the serial
2 presence detect includes receiving an indicator to indicate the data mask mapping scheme.
- 1 5. The method of claim 3, wherein said receiving the information from the serial
2 presence detect includes receiving the data mask mapping scheme.
- 1 6. The method of claim 1, wherein:
2 said obtaining includes writing at least one test data mask pattern and at least one
3 test data pattern to a range of memory in the memory module and reading at least one

4 resulting data pattern that was stored in the range of memory responsive to the at least one
5 test data pattern being modified by the at least one test data mask pattern; and

6 said determining includes determining a portion of the data mask mapping scheme
7 to be used for the range of memory based on the at least one resulting data pattern.

1 7. The method of claim 6, wherein said writing includes:

2 performing a first write transfer to write a first test data pattern to the range of
3 memory; and

4 performing a second write transfer to the range of memory, the second write
5 transfer including a second test data pattern and a test data mask pattern, the test data mask
6 pattern to not write-protect a particular data chunk in the second test data pattern.

1 8. An apparatus, comprising:

2 a memory controller having a hardwired selection device to program the memory
3 controller with a data mask mapping scheme, the data mask mapping scheme to associate
4 at least one data mask bit with at least one data chunk in a memory module; and

5 an output to be coupled to the memory module.

1 9. The apparatus of claim 8, wherein the hardwired selection device is to receive the
2 at least one data mask bit and at least a portion of the at least one data chunk.

1 10. The apparatus of claim 9, wherein the hardwired selection device is to select one of
2 the at least one data mask bit to be associated with one of the at least one data chunk
3 according to the data mask mapping scheme.

1 11. The apparatus of claim 8, wherein the hardwired selection device is to implement
2 the data mask mapping scheme.

1 12. An apparatus, comprising:
2 a memory controller including a storage device having information to indicate a
3 data mask mapping scheme for the memory controller; and
4 an output coupled to the memory module.

1 13. The apparatus of claim 12, wherein the storage device is loadable with the data
2 mask map by software.

1 14. The apparatus of claim 12, wherein the storage device is loadable with the data
2 mask map by BIOS.

1 15. The apparatus of claim 12, wherein the storage device is to include the information
2 at manufacture time.

1 16. The apparatus of claim 12, wherein the information is to include at least one
2 indicator to indicate the data mask mapping scheme.

1 17. The apparatus of claim 12, wherein the information is to include the data mask
2 mapping scheme.

1 18. A system, comprising:

2 a memory module to use at least one data mask mapping scheme to associate at
3 least one data mask bit with at least one data chunk;

4 a memory controller coupled with the memory module, the memory controller to
5 be programmed with the at least one data mask mapping scheme used in the memory
6 module.

1 19. The system of claim 18, wherein the memory module includes a first and a second
2 memory rank to use at least one of the at least one data mask mapping scheme.

1 20. The system of claim 19, wherein the first memory rank is to use a different data mask
2 mapping scheme than the second memory rank.

1 21. The system of claim 19, wherein the first memory rank is to use a same data mask
2 mapping scheme as the second memory rank.

1 22. The system of claim 18, wherein the memory controller is to include a storage device
2 to be programmed with one of the at least one data mask mapping scheme used in the
3 memory module.

1 23. The system of claim 22, wherein the storage device is to be coupled with a selection
2 device to select one of the at least one data mask bit to be associated with the at least one
3 data chunk according to the data mask mapping scheme.

1 24. A machine-readable medium that provides instructions, which when executed by a
2 machine, causes the machine to perform operations comprising:

3 obtaining, from within a memory system, information to indicate a data mask
4 mapping scheme to be used in a memory module in the memory system; and
5 determining the data mask mapping scheme based on the information.

1 25. The machine-readable medium of claim 24, wherein said obtaining includes:

2 sending at least one instruction to the memory module directing the memory
3 module to send the information; and
4 receiving the information from the memory module.

1 26. The machine-readable medium of claim 25, wherein said receiving the information
2 from the memory module includes receiving the information from a serial presence detect
3 within the memory module.

1 27. The machine-readable medium of claim 26, wherein said receiving the information
2 from the serial presence detect includes receiving an indicator to indicate the data mask
3 mapping scheme.

1 28. The machine-readable medium of claim 24, wherein:

2 said obtaining includes writing at least one test data mask pattern and at least one
3 test data pattern to a range of memory in the memory module and reading at least one
4 resulting data pattern that was stored in the range of memory responsive to the at least one
5 test data pattern being modified by the at least one test data mask pattern; and

6 said determining includes determining a portion of the data mask mapping scheme
7 to be used for the range of memory based on the at least one resulting data pattern.

1 29. The machine-readable medium of claim 28, wherein said writing includes:

2 performing a first write transfer to write a first test data pattern to the range of
3 memory; and

4 performing a second write transfer to the range of memory, the second write
5 transfer including a second test data pattern and a test data mask pattern, the test data mask
6 pattern to not write-protect a particular data chunk in the second test data pattern.

1 30. The machine-readable medium of claim 28, wherein said determining the portion of
2 the data mask mapping scheme includes identifying the particular data chunk in the second
3 test data pattern based on the at least one resulting data pattern.